Modern Very-Large-Scale Integrated (VLSI) Circuits and Systems

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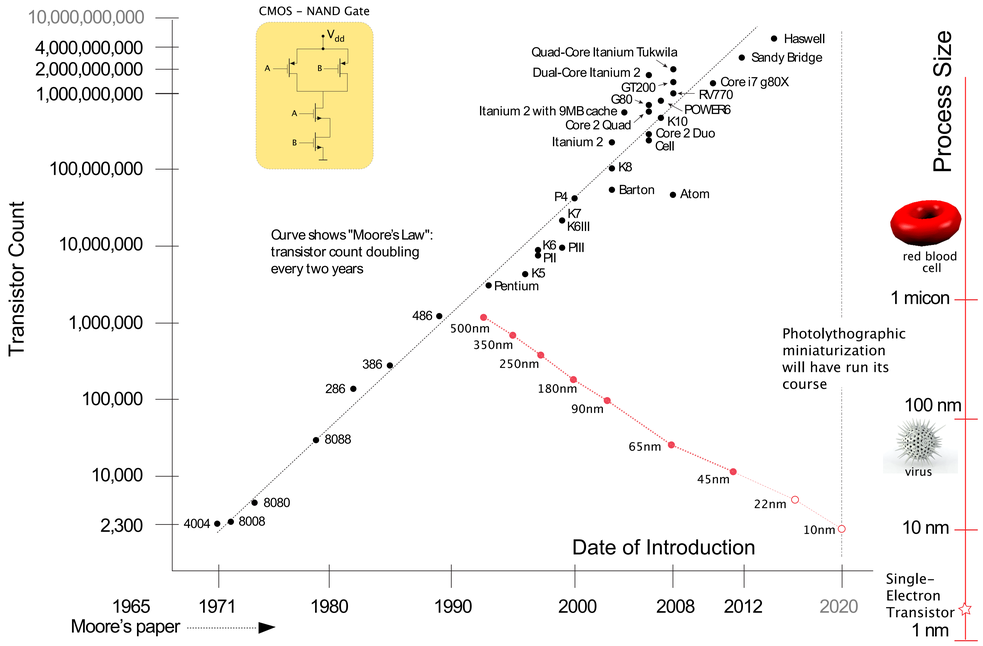
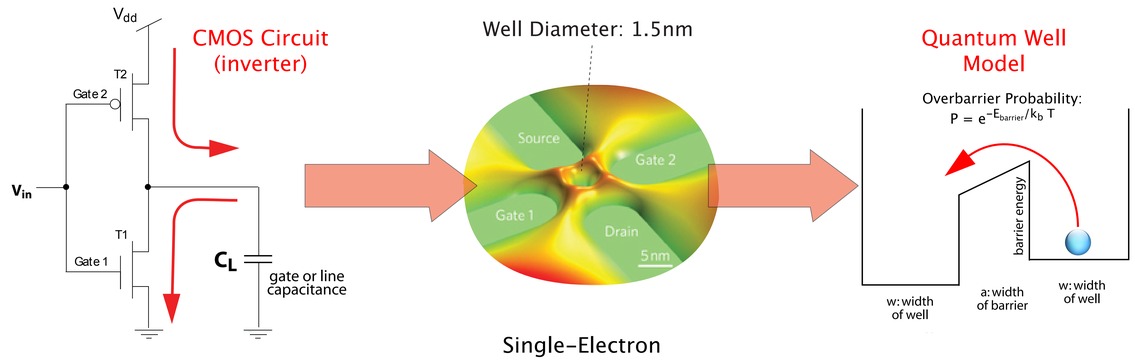
VLSI Development

The **International Technology Roadmap for Semiconductors** is a set of documents produced by a group of semiconductor industry experts, who represent the sponsoring organisations which include the Semiconductor Industry Associations of the US, Europe, Japan, South Korea and Taiwan. The ITRS represents the best opinion on the directions of research into areas of technology and time-lines up to about 15 years into the future. It predicts and quantifies major developments in the large scale systems integration field of technology.



Charged-Based Computation



Complementary Metal-Oxide Semiconductor

CMOS is the preferred technology today, since it allows for the massive miniaturization of integrated circuits we have observed over the last 5 decades.

A CMOS circuit is a digital switch which stores information by charging and discharging a capacitive load C_L (charge-based computation). Each computational cycle costs an amount of energy equal to:

$$C_L V_{dd}^2 \text{ [Joules]}$$

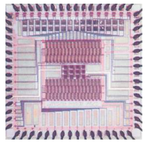
Limits of Charge-Based Computation

is achieved if a single quantum charge (electron) is used as information carrier. Such devices have been built in the lab, but **not** at minimal energy levels (see graphic middle above).

The minimal energy required to distinguish a charge trapped in a double well (right side) is given by the Landauer limit for irreversible computing (1961) given as

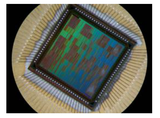
$$E_L = k_b T \ln 2 = 0.017\text{eV} \quad [2.72 \text{ zepto Joules}]$$

The Laundauer limit has been verified experimentally! It is not practical since minimum energy cells are at the limit of distinguishability -the overbarrier probability reaches 50%.

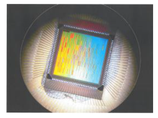


Analog Turbo Decoder in CMOS p35 μm

Some VLSI circuits built in our laboratory:



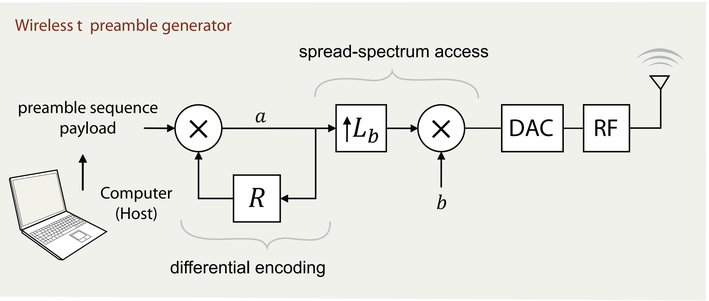
Digital Convolutional LDPCDecoder in CMOS 180 μm process, 175Mbps, 10^{-3} BER at 3dB SNR, 14.4 mm^2 area

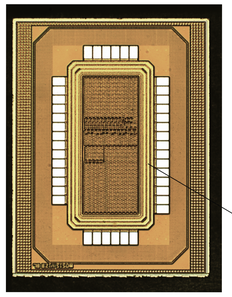


Bit-Serial LDPC Decoder in CMOS p18 μm process, 250 Mbps, 11 mm^2 area

Future Challenges:

1. Control leakage currents that dominate the stand-by power of smaller processes.
2. Reduce power consumption of indvidual gates so higher levels of integration are possible, expected to be limited by heat transport limitations.
3. Subthreshold, asynchronous design, and mixed analog-digital design tools and methodologies to produce power optimized VLSI solutions.





130 nm digital packet transmitter implemented by Graduate Student Malihe Ahmadi in 2012.

Complex Systems
are nowadays routinely implemented in VLSI circuits, executing a myriad of complex tasks.

Commercial highly integrated VLSI circuit to implement the IEEE 802.3an standard for 10Gbit/s communications over twisted pair copper cables. The chip contains a highly complex communications system and uses more then 10,000,000 transistors.

To Probe Further:

G.~Cheng et.al., "Sketched oxide single-electron transistor," Nature Nanotechnology 6, 343--347 (2011) doi:10.1038/nnano.2011.56.

V.~Zhirnov et.al., "Limits to binary logic switch scaling -- A gedanken model," Proceedings of the IEEE, Vol.~91, No.~11, November 2003.

J.D.~Meindl and J.A.~Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," IEEE J.~Solid-State Circuits, Vol.~35, No.~10, October 2000.

R. Landauer, "Irreversibility and heat generation in the computing process," IBM J. Research and Development, vol. 5, pp. 181-191, 1961.